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| 10/708,316 | 02/24/2004 | Zachary E. Berndlmaier | BUR920030156US1 | 2315 |

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| EXAMINER | |
|---|---|
| SIDDIQUI, SAQIB JAVAID | |
| **ART UNIT** | **PAPER NUMBER** |
| 2138 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 02/16/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/708,316 | BERNDLMAIER ET AL. | |
| | Examiner | Art Unit | |
| | Saqib J. Siddiqui | 2138 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Applicant's response was received and entered October 16, 2006.

- Claims 1-28 are pending.
- Application is currently pending.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-3, 7-10, 14-17, 21-24 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Waite US Pat no. 5,157,664.

As per claims 1, 8, 15 and 22:

Waite teaches an autonomously self-monitoring (Figure 1 # 10) and self-correcting (Figure 1 # 10) integrated circuit device and a method of adjusting operation of an integrated device comprising: a self-testing controller (Figure 2 # 22, column 5, lines 15-21) adapted to periodically perform performance self-testing on said integrated circuit device; a comparator adapted to evaluate whether results from said self-testing are within acceptable limits (Figure 1 # 42); and a processor adapted to permanently (once fuse is blown or activated for redundant columns or rows) adjust parameters of

said integrated circuit device until said results from said self-testing are within said acceptable limits (column 2, lines 60-67).

As per claims 2, 9, 16 and 23:

Waite teaches the autonomously self-monitoring (Figure 1 # 10) and self-correcting (Figure 1 # 10) integrated circuit device and a method of adjusting operation of an integrated device as rejected in claim 1 above, wherein said performance self-testing comprises one or more of a built-in self test (BIST) unit (Figure 2 # 26) and a functional testing unit (abstract).

As per claims 3, 10, 17 and 24:

Waite teaches the autonomously self-monitoring (Figure 1 # 10) and self-correcting (Figure 1 # 10) integrated circuit device and a method of adjusting operation of an integrated device as rejected in claim 2 above, wherein said functional testing unit is adapted to apply functional test sequences (abstract) to said integrated circuit device until failure (Figure 1 # 34), and said comparator compares the failure frequency against predetermined limits (column 4, lines 10-40).

As per claims 7, 14, 21 and 28:

Waite teaches the autonomously self-monitoring (Figure 1 # 10) and self-correcting (Figure 1 # 10) integrated circuit device and a method of adjusting operation of an integrated device as rejected in claim 1 above, further comprising a permanent storage device adapted to maintain a history of adjustments made to said parameters by said processor (column 3, lines 30-65).

Claims 1-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Zorian et al. US Pat no. 7,127,647 B1.

As per claims 1, 8, 15 and 22:

Zorian et al. teaches an autonomously self-monitoring (Figure 1 # 108) and self-correcting (Figure 1 # 108) integrated circuit device and a method of adjusting operation of an integrated device comprising: a self-testing controller (Figure 3 "BIST") adapted to periodically perform performance self-testing on said integrated circuit device (column 5, lines 5-25); a comparator adapted to evaluate whether results from said self-testing are within acceptable limits (column 6, lines 5-35); and a processor adapted to permanently (once fuse is blown or activated for redundant columns or rows) adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (column 7, lines 20-45).

As per claims 2, 9, 16 and 23:

Zorian et al. teaches the autonomously self-monitoring (Figure 1 # 108) and self-correcting (Figure 1 # 108) integrated circuit device and a method of adjusting operation of an integrated device as rejected in claim 1 above, wherein said performance self-testing comprises one or more of a built-in self test (BIST) unit (Figure 3 "BIST") and a functional testing unit (column 6, lines 20-25).

As per claims 3, 10, 17 and 24:

Zorian et al. teaches the autonomously self-monitoring (Figure 1 # 108) and self-correcting (Figure 1 # 108) integrated circuit device and a method of adjusting operation of an integrated device as rejected in claim 2 above, wherein said functional testing unit

is adapted to apply functional test sequences (column 6, lines 20-25) to said integrated circuit device until failure (Figure 1 # 34), and said comparator compares the failure frequency against predetermined limits (Figure 8 # 802).

As per claims 4, 6, 11, 13, 18, 20, 25 and 27:

Zorian et al. teaches the autonomously self-monitoring (Figure 1 # 108) and self-correcting (Figure 1 # 108) integrated circuit device and a method of adjusting operation of an integrated device as rejected in claim 1 above, wherein said processor adjusts said parameters by altering the voltage supplied to portions of said integrated circuit by using voltage regulators (column 4, lines 50-65).

As per claims 5, 12, 19, and 26:

Zorian et al. teaches the autonomously self-monitoring (Figure 1 # 108) and self-correcting (Figure 1 # 108) integrated circuit device and a method of adjusting operation of an integrated device as rejected in claim 1 above, further comprising activating electronic fuses permanently (Figure 2 # 218).

As per claims 7, 14, 21 and 28:

Zorian et al. teaches the autonomously self-monitoring (Figure 1 # 108) and self-correcting (Figure 1 # 108) integrated circuit device and a method of adjusting operation of an integrated device as rejected in claim 1 above, further comprising a permanent storage device adapted to maintain a history of adjustments made to said parameters by said processor (Figure 4).

Claims 1-28 are rejected under 35 U.S.C. 102(e) as being anticipated by McBride US Pat no. 6,829,737.

As per claims 1, 8, 15 and 22:

McBride teaches an autonomously self-monitoring (Figure 1 # 108) and self-correcting (Figure 1) integrated circuit device and a method of adjusting operation of an integrated device comprising: a self-testing controller (Figure 3) adapted to periodically perform performance self-testing on said integrated circuit device (column 5, lines 5-25); a comparator adapted to evaluate whether results from said self-testing are within acceptable limits (column 6, lines 5-35); and a processor adapted to permanently (once fuse is blown or activated for redundant columns or rows) adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (column 7, lines 20-45).

As per claims 2, 9, 16 and 23:

McBride teaches the autonomously self-monitoring (Figure 1) and self-correcting (Figure 1) integrated circuit device and a method of adjusting operation of an integrated device as rejected in claim 1 above, wherein said performance self-testing comprises one or more of a built-in self test (BIST) unit (Figure 3 "BIST") and a functional testing unit (column 6, lines 20-25).

As per claims 3, 10, 17 and 24:

McBride teaches the autonomously self-monitoring (Figure 1) and self-correcting (Figure 1) integrated circuit device and a method of adjusting operation of an integrated device as rejected in claim 2 above, wherein said functional testing unit is adapted to apply functional test sequences (column 6, lines 20-25) to said integrated circuit device

until failure (Figure 1 # 34), and said comparator compares the failure frequency against predetermined limits (Figure 8 # 802).

As per claims 4, 6, 11, 13, 18, 20, 25 and 27:

McBride teaches the autonomously self-monitoring (Figure 1) and self-correcting (Figure 1) integrated circuit device and a method of adjusting operation of an integrated device as rejected in claim 1 above, wherein said processor adjusts said parameters by altering the voltage supplied to portions of said integrated circuit by using voltage regulators (column 4, lines 50-65).

As per claims 5, 12, 19, and 26:

McBride teaches the autonomously self-monitoring (Figure 1) and self-correcting (Figure 1) integrated circuit device and a method of adjusting operation of an integrated device as rejected in claim 1 above, further comprising activating electronic fuses permanently (Figure 2).

As per claims 7, 14, 21 and 28:

McBride teaches the autonomously self-monitoring (Figure 1) and self-correcting (Figure 1) integrated circuit device and a method of adjusting operation of an integrated device as rejected in claim 1 above, further comprising a permanent storage device adapted to maintain a history of adjustments made to said parameters by said processor (Figure 4).

***Claim Rejections - 35 USC § 103***

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 4-6, 11-13, 18-20 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waite US Pat no. 5,157,664, and further in view of Bartlett et al. US Pat no. 3,761,882.

As per claims 4-6, 11-13, 18-20 and 25-27:

Waite substantially teaches an autonomously self-monitoring (Figure 1 # 10) and self-correcting (Figure 1 # 10) integrated circuit device and a method of adjusting operation of an integrated device comprising: a self-testing controller (Figure 2 # 22, column 5, lines 15-21) adapted to periodically perform performance self-testing on said integrated circuit device; a comparator adapted to evaluate whether results from said self-testing are within acceptable limits (Figure 1 # 42); and a processor adapted to permanently (once fuse is blown or activated for redundant columns or rows) adjust parameters of said integrated circuit device until said results from said self-testing are within said acceptable limits (column 2, lines 60-67).

Waite does not explicitly teach the integrated circuit, further comprising electronic fuses and voltage regulators.

However, Bartlett et al. in an analogous art teaches the integrated circuit, further comprising electronic fuses wherein said processor is adapted to activate said electronic fuses to permanently change said parameters of said integrated circuit device (column 19, lines 4-15). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to understand that Waite is in fact changing voltage and activating fuses during replacement of memories, as it is a well known method used to replace faulty devices with redundant memories.

**Examiner's Note:** Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

Saqib Siddiqui
Art Unit 2138
02/06/2007

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